REMARKS

Claims 1-26 and 49-55 are currently in the application for further prosecution. Claims 27-48 have been canceled without prejudice in response to the previous restriction requirement. By this amendment, Claims 1, 4, 10-11, 20-22, 26, 49-50, 52 and 54 have been amended. New claim 55 has been added.

The Office Action objected to claims 10, 20 and 54 for various informalities. Applicant has amended these claims in accordance with the suggestions of the Examiner and respectfully submits that the objections be withdrawn.

The Office Action rejected claims 1, 7, 9, 11, 13, 15, 21 and 22-25 as anticipated by U.S. Patent No. 7,142,731 ("Toi"). Claims 8, 10, 14, 17-20, 26, 49 and 52-54 are rejected under 35 U.S.C. 103 as being obvious over Toi. Claims 2-6, 12 and 50-51 are rejected under 35 U.S.C. 103 as obvious over Toi in view of U.S. Patent No. 6,788,212 ("Deng"). Claim 16 is rejected under 35 U.S.C. 103 as obvious over Toi in view of U.S. Patent No. 5,754,227 ("Fukuoka").

The present claims are generally directed toward a digital imaging apparatus that has an optical sensor and analog to digital converter to convert a detected image to digital image information. A plurality of computational elements with a first computational element having a first fixed architecture and a second computational element having a second different fixed architecture is provided. An interconnection network having interconnections coupled to each of the plurality of computational elements allows the configuration of the computational elements for performance of a first imaging function. The configuration is performed in response to first configuration information via the interconnections between the first and second computational elements. The plurality of computational elements is reconfigured for performance of a second

imaging function in response to second configuration information changing the interconnections between the computational elements.

Toi Does Not Disclose Heterogeneous Computing Elements

Independent claims 1 and 49 require "a first computational element of the plurality of computational elements having a first fixed architecture and a second computational element of the plurality of computational elements having a second fixed architecture, the first fixed architecture being different than the second fixed architecture." Thus, the image processing functions are performed by basic fixed, heterogeneous (different fixed architectures each dedicated to specialized computing functions) computational elements that may be reconnected via the interconnection network to configure the computational elements to perform an imaging function. The advantage of using the novel computational elements with different heterogeneous architectures over known homogeneous field programmable gate arrays (FPGA) such as that used in Toi is greater speed and resource efficiency. Homogeneous computational elements require more integrated circuit area, time and power than the heterogeneous circuits. Also, in order to configure the prior art homogeneous gates, an extensive interconnect network must be used with a resulting high capacitance causing slow operation and high power consumption. Further such FPGAs are subject to chaotic routing thus resulting in delay and wasted logic resources. In fact, the specification explains:

> The third and perhaps most significant concept of the present invention, and a marked departure from the concepts and precepts of the prior art, is the concept of reconfigurable "heterogeneity" utilized to implement the various selected algorithms mentioned above. As indicated above, prior art reconfigurability has relied exclusively on homogeneous FPGAs, in which identical blocks of logic gates are repeated as an array within a rich, programmable interconnect, with the interconnect subsequently configured to provide connections between and among the identical gates to implement a particular function, albeit inefficiently and often with routing and combinatorial problems.

(p. 12, l. 28 to p. 13, l. 4).

Applicant has amended claims 1 and 49 to require "heterogeneous" computational elements. Toi relies on prior art homogeneous computational elements organized in an FPGA 106 to perform two or more different image processing functions in accordance with internal logic descriptions. The FPGA 106 in Toi is configured between a first internal logic description and a second internal logic description to perform different imaging functions as shown in Figs. 4-6. The Office Action has equated the plurality of computational units having a fixed architecture as circuits 400, 401 and 402 (that are FPGA configured logic for the black balance function) and a second computational element having a second fixed architecture as the FPGA configured logic for pixel interpolation. (p. 3). The Office Action has misinterpreted Toi, since the FPGA 106 must be programmed to configure identical, homogeneous, logic elements to perform different functions. The different groups of computational elements do not have different fixed architectures as the Office Action asserts, rather the computational elements in Toi are composed of identical gates that make up the FPGA 106. The identical gates are configured into different computational groups to perform different functions but the gates have the same identical fixed architecture. The present claims are therefore allowable over Toi, because Toi does not disclose nor teach heterogeneous computational elements including computational elements with first and second different fixed architectures.

Toi Does Not Disclose An Interconnection Network Configuring Interconnections To Configure the Computing Elements

A second feature that distinguishes the present claims from Toi is the use of configuring and reconfiguring interconnections of the interconnect network between the computational elements to configure the computational elements. In order to further distinguish Toi, Applicant has amended claims 1 and 49 to require that the interconnection network configures

interconnections between computational elements and that the computational elements are reconfigured by reconfiguration the interconnections between them. Toi does not disclose any of these features. First, the Office Action cannot cite to any physical element in Toi that serves as an interconnection network. The Office Action asserts that Toi includes "an interconnection network (network that allows the computation elements in field programmable gate array 106 to operate in parallel)" but fails to note any section of Toi or drawing that shows an interconnection network. To the extent that such an interconnection network exists, it does not have interconnections between computational elements. Further, there is no disclosure nor suggestion that the configuration information causes configuration by configuring the interconnections in the interconnection network between the computational elements. Applicant respectfully submits that claims 1 and 49 and their dependents are allowable over Toi.

New Claim 55 Is Allowable Over Toi

Applicant has added new claim 55. New claim 55 is a method claim that incorporates the elements of an interconnection network causes configuration by configuring the interconnections in the interconnection network between the computational elements. As such new claim 55 is allowable over Toi.

Conclusion

It is Applicant's belief that all of the claims are now in condition for allowance and actions towards that effect is respectfully requested.

If there are any matters which may be resolved or clarified through a telephone interview, the Examiner is respectfully requested to contact the undersigned attorney at the number indicated.

Respectfully submitted,

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